

# Claims

- [c1] 1. A circuit comprising:
- a reference buffer providing a first voltage signal on an output terminal;
  - a capacitor having a large capacitance connected to a first node;
  - an analog-to-digital converter (ADC) implemented using switched capacitors, said ADC receiving a reference signal from said first node; and
  - a resistor connecting said output terminal to said first node, whereby said reference signal is generated from said first voltage signal, whereby said resistor minimizes a droop which may otherwise be presented in said reference signal.
- [c2] 2. The circuit of claim 1, wherein a resistance value of said resistor substantially equals  $(A+B+C)$ , wherein A equals a resistance present between said capacitor and said first node, B equals an output resistance of said reference buffer, and C equals a routing resistance between said output terminal and said first node.
- [c3] 3. The circuit of claim 2, wherein said reference buffer comprises an operational amplifier having two input ter-

minals and said output terminal, wherein said B equals output resistance of said operational amplifier.

[c4] 4. The circuit of claim 3, wherein said two input terminals comprise an inverting terminal and a non-inverting terminal, one of said two input terminals being connected to a voltage source.

[c5] 5. The circuit of claim 2, wherein said ADC and said reference buffer are provided on an integrated circuit, said capacitor being provided external to said integrated circuit and being connected to said integrated circuit by a bond pad using a pin, said A containing a sum of resistance values of resistance associated with said capacitor, resistance of the routing path between said pin and said capacitor, resistance of said pin, resistance of the routing path between said pin and said bond pad, and resistance of said bond pad.

[c6] 6. A device comprising:  
a reference buffer providing a first voltage signal on an output terminal;  
a capacitor having a large capacitance connected to a first node;  
an analog-to-digital converter (ADC) implemented using switched capacitors, said ADC receiving a reference signal from said first node;

a resistor connecting said output terminal to said first node, whereby said reference signal is generated from said first voltage signal, whereby said resistor minimizes a droop which may otherwise be presented in said reference signal; and  
a processing block processing said digital code.

- [c7] 7. The device of claim 6, wherein said device comprises a camera, said camera further comprising:  
a lens for focusing light signal reflected by an object;  
a charge coupled device (CCD) storing charges based on the intensity of said light signal in a plurality of pixels corresponding to said object; and  
a correlated double sampler (CDS) generating voltage levels corresponding to said plurality of pixels, wherein said voltage levels are sampled by said ADC.
- [c8] 8. The camera of claim 7, wherein said reference buffer and said ADC is implemented in an integrated circuit (IC).
- [c9] 9. The device of claim 6, wherein a resistance value of said resistor substantially equals  $(A+B+C)$ , wherein A equals a resistance present between said capacitor and said first node, B equals an output resistance of said reference buffer, and C equals a routing resistance between said output terminal and said first node.

- [c10] 10. The device of claim 6, wherein said reference buffer comprises an operational amplifier having two input terminals and said output terminal, wherein said B equals output resistance of said operational amplifier.
- [c11] 11. The circuit of claim 10, wherein said two input terminals comprise an inverting terminal and a non-inverting terminal, one of said two input terminals being connected to a voltage source.
- [c12] 12. The circuit of claim 6, wherein said ADC and said reference buffer are provided on an integrated circuit, said capacitor being provided external to said integrated circuit and being connected to said integrated circuit by a bond pad using a pin, said A containing a sum of resistance values of resistance associated with said capacitor, resistance of the routing path between said pin and said capacitor, resistance of said pin, resistance of the routing path between said pin and said bond pad, and resistance of said bond pad.